	L #	Hits	Search Text	DBs
1	L1	19226	(instruction prefetch$3 fetch$3) near10 (buffer queue)	USPAT; US-PGPUB
2	L2	53755	(combin$3 complex) near5 (operation instruction)	USPAT; US-PGPUB
3	L4	6994	(instruction prefetch$3 fetch$3) near10 (buffer queue)	EPO; JPO; DERWENT; IBM_TDB
4	L5	11748	(combin$3 complex) near5 (operation instruction)	EPO; JPO; DERWENT; IBM_TDB
5	L3	201	1 near30 2	USPAT; US-PGPUB
6	L6	16	4 near50 5	EPO; JPO; DERWENT; IBM_TDB
7	L9	202	1 near99 2	USPAT; US-PGPUB
8	L10	16	4 near99 5	EPO; JPO; DERWENT; IBM_TDB
9	L12	3627	(merg$3) near5 (operation instruction)	USPAT; US-PGPUB
10	L14	515	(merg$3) near5 (operation instruction)	EPO; JPO; DERWENT; IBM_TDB
11	L15	7	4 near50 14	EPO; JPO; DERWENT; IBM_TDB
12	L13	87	1 near30 12	USPAT; US-PGPUB
13	L16	87	1 near99 12	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20030074542 A1	☐	Multiprocessor system and program optimizing method	712/20
2	US 20030053170 A1	☐	Optoelectronic device capable of participating in in-band traffic	398/139
3	US 20020114395 A1	☐	SYSTEM METHOD AND APPARATUS FOR A MOTION COMPENSATION INSTRUCTION GENERATOR	375/240.18
4	US 20020087806 A1	☐	Cache coherence protocol engine and method for efficient processing of interleaved memory transactions in a multiprocessor system	711/141
5	US 20020078285 A1	☐	Reduction of interrupts in remote procedure calls	710/260
6	US 20020057446 A1	☐	MULTI- INSTRUCTION STREAM PROCESSOR	358/1.13
7	US 20020050992 A1	☐	Geometry instructions for graphics data compression	345/423
8	US 20020034252 A1	☐	System, method and apparatus for an instruction driven digital video processor	375/240.17
9	US 20010050682 A1	☐	Decompression of variable-length encoded compressed three-dimensional graphics data	345/420
10	US 20010021971 A1	☐	SYSTEM FOR EXECUTING INSTRUCTIONS HAVING FLAG FOR INDICATING DIRECT OR INDIRECT SPECIFICATION OF A LENGTH OF OPERAND DATA	712/215
11	US 6675287 B1	☐	Method and apparatus for store forwarding using a response buffer data path in a write-allocate-configurable microprocessor	712/216
12	US 6674536 B2	☐	Multi-instruction stream processor	358/1.15
13	US 6643745 B1	☐	Method and apparatus for prefetching data into cache	711/138
14	US 6622218 B2	☐	Cache coherence protocol engine and method for efficient processing of interleaved memory transactions in a multiprocessor system	711/141
15	US 6603470 B1	☐	Compression of surface normals in three-dimensional graphics data	345/419
16	US 6532012 B2	☐	Geometry instructions for graphics data compression	345/423
17	US 6525722 B1	☐	Geometry compression for regular and irregular mesh structures	345/419
18	US 6522327 B2	☐	Decompression of variable-length encoded compressed three-dimensional graphics data	345/428
19	US 6522326 B1	☐	Decompression of quantized compressed three-dimensional graphics data	345/427

	Document ID	U	Title	Current OR
20	US 6507898 B1	☐	Reconfigurable data cache controller	711/168
21	US 6490324 B1	☐	System, method and apparatus for a variable output video decoder	375/240.25
22	US 6477640 B1	☐	Apparatus and method for predicting multiple branches and performing out-of-order branch resolution	712/238
23	US 6463525 B1	☐	Merging single precision floating point operands	712/222
24	US 6421696 B1	☐	System and method for high speed execution of Fast Fourier Transforms utilizing SIMD instructions on a general purpose processor	708/404
25	US 6414996 B1	☐	System, method and apparatus for an instruction driven digital video processor	375/240.17
26	US 6414687 B1	☐	Register setting-micro programming system	345/503
27	US 6396504 B1	☐	Graphical image data reformatting method and apparatus	345/589
28	US 6393549 B1	☐	Instruction alignment unit for routing variable byte-length instructions	712/204
29	US 6393545 B1	☐	Method apparatus and system for managing virtual memory with virtual-physical mapping	712/34
30	US 6351801 B1	☐	Program counter update mechanism	712/205
31	US 6349379 B1	☐	System for executing instructions having flag for indicating direct or indirect specification of a length of operand data	712/210
32	US 6336180 B1	☐	Method, apparatus and system for managing virtual memory with virtual-physical mapping	712/34
33	US 6336168 B1	☐	System and method for merging multiple outstanding load miss instructions	711/141
34	US 6321303 B1	☐	Dynamically modifying queued transactions in a cache memory system	711/140
35	US 6311258 B1	☐	Data buffer apparatus and method for storing graphical data using data encoders and decoders	711/200
36	US 6311254 B1	☐	Multiple store miss handling in a cache memory memory system	711/126
37	US 6307557 B1	☐	Decompression of three-dimensional graphics data including quantization, delta-encoding, and variable-length encoding	345/428
38	US 6289138 B1	☐	General image processor	382/307
39	US 6275921 B1	☐	Data processing device to compress and decompress VLIW instructions by selectively storing non-branch NOP instructions	712/24
40	US 6272624 B1	☐	Method and apparatus for predicting multiple conditional branches	712/239
41	US 6272257 B1	☐	Decoder of variable length codes	382/246
42	US 6269427 B1	☐	Multiple load miss handling in a cache memory system	711/140

	Document ID	U	Title	Current OR
43	US 6259456 B1	☐	Data normalization techniques	345/619
44	US 6246396 B1	☐	Cached color conversion method and apparatus	345/604
45	US 6239805 B1	☐	Method and apparatus for geometric compression of three-dimensional graphics data	345/419
46	US 6237085 B1	☐	Processor and method for generating less than (LT), Greater than (GT), and equal to (EQ) condition code bits concurrent with a logical or complex operation	712/223
47	US 6237083 B1	☐	Microprocessor including multiple register files mapped to the same logical storage and inhibiting sychronization between the register files responsive to inclusion of an instruction in an instruction sequence	712/217
48	US 6237079 B1	☐	Coprocessor interface having pending instructions queue and clean-up queue and dynamically allocating memory	712/34
49	US 6195674 B1	☐	Fast DCT apparatus	708/402
50	US 6157998 A	☐	Method for performing branch prediction and resolution of two or more branch instructions within two or more branch prediction buffers	712/238
51	US 6141734 A	☐	Method and apparatus for optimizing the performance of LDxL and STxC interlock instructions in the context of a write invalidate protocol	711/144
52	US 6118724 A	☐	Memory controller architecture	365/230.05
53	US 6088034 A	☐	Decompression of surface normals in three-dimensional graphics data	345/420
54	US 6061749 A	☐	Transformation of a first dataword received from a FIFO into an input register and subsequent dataword from the FIFO into a normalized output dataword	710/65
55	US 6049390 A	☐	Compressed merging of raster images for high speed digital printing	358/1.15
56	US 6047369 A	☐	Flag renaming and flag masks within register alias table	712/217
57	US 6035390 A	☐	Method and apparatus for generating and logically combining less than (LT), greater than (GT), and equal to (EQ) condition code bits concurrently with the execution of an arithmetic or logical operation	712/220
58	US 6035387 A	☐	System for packing variable length instructions into fixed length blocks with indications of instruction beginning, ending, and offset within block	712/210
59	US 6035386 A	☐	Program counter update mechanism	712/205
60	US 6028610 A	☐	Geometry instructions for decompression of three-dimensional graphics data	345/501
61	US 5948100 A	☐	Branch prediction and fetch mechanism for variable length instruction, superscalar pipelined processor	712/238
62	US 5933353 A	☐	Mesh buffer for decompression of compressed three-dimensional graphics data	345/501
63	US 5905502 A	☐	Compression of three-dimensional graphics data using a generalized triangle mesh format utilizing a mesh buffer	345/420
64	US 5870094 A	☐	System and method for transferring compressed three-dimensional graphics data	345/419

	Document ID	U	Title	Current OR
65	US 5867167 A	☐	Compression of three-dimensional graphics data including quantization, delta-encoding, and variable-length encoding	345/419
66	US 5860107 A	☐	Processor and method for store gathering through merged store operations	711/140
67	US 5854913 A	☐	Microprocessor with an architecture mode control capable of supporting extensions of two distinct instruction-set architectures	712/210
68	US 5842004 A	☐	Method and apparatus for decompression of compressed geometric three-dimensional graphics data	345/501
69	US 5805878 A	☐	Method and apparatus for generating branch predictions for multiple branch instructions indexed by a single instruction pointer	712/239
70	US 5799162 A	☐	Program counter update mechanism	712/205
71	US 5793371 A	☐	Method and apparatus for geometric compression of three-dimensional graphics data	345/418
72	US 5748932 A	☐	Cache memory system for dynamically altering single cache memory line as either branch target entry or prefetch instruction queue based upon instruction sequence	715/526
73	US 5659733 A	☐	Sort processing method and apparatus for sorting data blocks using work buffer merge data records while sequentially transferring data records from work buffers	707/7
74	US 5559975 A	☐	Program counter update mechanism	712/230
75	US 5268995 A	☐	Method for executing graphics Z-compare and pixel merge instructions in a data processor	345/422
76	US 5230068 A	☐	Cache memory system for dynamically altering single cache memory line as either branch target entry or pre-fetch instruction queue based upon instruction sequence	711/137
77	US 5202972 A	☐	Store buffer apparatus in a multiprocessor system	711/123
78	US 5197145 A	☐	Buffer storage system using parallel buffer storage units and move-out buffer registers	711/143
79	US 5167026 A	☐	Simultaneously or sequentially decoding multiple specifiers of a variable length pipeline instruction based on detection of modified value of specifier registers	712/210
80	US 5157388 A	☐	Method and apparatus for graphics data interpolation	345/673
81	US 5148528 A	☐	Method and apparatus for simultaneously decoding three operands in a variable length instruction when one of the operands is also of variable length	712/210
82	US 5142633 A	☐	Preprocessing implied specifiers in a pipelined processor	712/225
83	US 5113515 A	☐	Virtual instruction cache system using length responsive decoded instruction shifting and merging with prefetch buffer outputs to fill instruction buffer	711/125
84	US 5081698 A	☐	Method and apparatus for graphics display data manipulation	345/422
85	US 4890220 A	☐	Vector processing apparatus for incrementing indices of vector operands of different length according to arithmetic operation results	712/8
86	US 4638429 A	☐	Data processing apparatus for processing operand store conflict	712/218
87	US 4497023 A	☐	Linked list of timed and untimed commands	712/205

	Document ID	U	Title	Current OR
1	JP 06290 208 A	☐	VECTOR PROCESSOR	
2	JP 05197 609 A	☐	STORE BUFFER MANAGING SYSTEM	
3	JP 04112 328 A	☐	DEGENERATION CONTROL SYSTEM FOR STORE INSTRUCTION	
4	JP 02156 349 A	☐	MEMORY CONTROLLER	
5	EP 99289 3 A	☐	Processor for executing instructions in parallel has instruction buffer and decoders storing and decoding two instructions and arbitration and merge logic arbitrating between instructions	
6	US 52689 95 A	☐	Executing method for graphics Z-compare and pixel merge instructions in data processor - involves using pixel compare result vector to selectively store pixels in image buffer according to pixel merge instruction	
7	US 52300 68 A	☐	Integrated instruction-queue and branch-target cache memory - has up to three active instruction queues each associated with sequential instruction stream started by control transfer instruction	